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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,756	10/07/2003	Michael J. Boudreaux	BUR920020077US1	5216
30449	7590	12/20/2005	EXAMINER	
SCHMEISER, OLSEN + WATTS 3 LEAR JET LANE SUITE 201 LATHAM, NY 12110			TAN, VIBOL	
		ART UNIT	PAPER NUMBER	
			2819	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/680,756	BOUDREAU ET AL. <i>(initials)</i>	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 07 October 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-20 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____. |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>10/7/04</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 6, 11-15 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Lindsay et al. (U.S. Pat. 6,677,778).

In claim 1, Lindsey et al. teaches all claimed features in Fig. 1, a semiconductor device comprising: a transmitter (within 11), receiver (within 12), and transmission line (130) formed within the semiconductor device, wherein the transmitter, receiver, and transmission line are adapted to control data transfer (signal) between a first core (11) and a second core (12) within the semiconductor device, wherein the transmitter is adapted to send a signal (data) over the transmission line (130) to the receiver adapted to receive the signal, *wherein* the receiver is further adapted to create (131) an impedance mismatch (reflection) to indicate that the second core is unable to transfer the data, and wherein the transmitter is adapted to detect the impedance mismatch (the reflection).

In claims 2 and 3, Lindsey et al. further teaches the semiconductor device of claim 1, wherein the receiver is further adapted to change an impedance (131) of the transmission

line to create the impedance mismatch (reflection); and wherein the receiver comprises a capacitor (Fig. 2) adapted to change the impedance of the transmission line.

In claim 4, Lindsey et al. further teaches the semiconductor device of claim 1, wherein the transmitter (within 11) is further adapted to terminate the data transfer upon (102 is open when 101 is closed to terminate; col. 2, lines31-33) detection of the impedance mismatch.

In claim 6, Lindsey et al. further teaches the semiconductor device of claim 1, wherein the signal is a voltage signal (inherent), and wherein the transmitter is adapted (inherent) to receive a reflection of the voltage signal.

Method claims 11-15 and 19 correspond to detailed circuitry already discussed similarly with regard to claims 1-4 and 6.

In claim 19, Lindsay et al. further teaches the method of claim 11 further comprising: creating by the receiver, an impedance mismatch (reflection created by 131) to indicate that the second core (12) is able to transfer the data between the first core and the second core; and detecting by the transmitter, the impedance match (reflection).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 5 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lindsay et al.

In claim 5, Lindsay et al. teaches all claimed features the semiconductor of claim 1; with the exception of showing the first core and the second core are each selected from the group consisting of a microcontroller, a microprocessor, and an integrated circuit. However, it is obvious to have selected the first core and second core are each selected from the group consisting of a microcontroller, a microprocessor, and an integrated circuit because the device of Lindsay et al. pertains to bidirectional data flow along a transmission line between a first and second semiconductor chips is capable to be employed in a microcontroller, a microprocessor, and an integrated circuit, as claimed in the present invention.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to implement the teachings of Lindsay et al. in the group consisting of a microcontroller, a microprocessor, and an integrated circuit in order to cause a false data value to be correctly seen as the proper data value during data communication.

Claim 20 corresponds to detailed circuitry already discussed similarly with regard to claim 5.

5. Claims 7-10 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lindsay et al. in view of Martin et al. (U. S. PAT. 6,639,423).

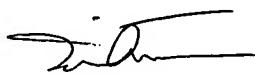
In claim 7, Lindsay et al. teaches all claimed features the semiconductor of claim 1; with the exception wherein the transmitter comprises a voltage comparator adapted to compare an amplitude of the voltage signal to an amplitude of the reflection of the voltage signal. However, Martin et al. teaching in Fig. 1, the transmitter (124) comprises

a voltage comparator (140) adapted to compare an amplitude (+148) of the voltage signal to an amplitude of the reflection of the voltage signal (+input for 140).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Lindsay et al. with the teachings of Martin et al. in order for the variable termination impedance to be modified in response to the comparison.

In claims 8-10, Lindsay et al. further teaches the semiconductor in claim 7, wherein the voltage comparator (140) is further adapted generate a control signal (feed into 122) and transmit the control signal to the first core (123); wherein the control signal is an enable signal (125) adapted to enable the data transfer between the first core (123) and the second core (173); and wherein the control signal is a disable signal (127) adapted to disable the data transfer between the first core and the second core.

Claims 16-18 correspond to detailed circuitry already discussed similarly with regard to claims 7-10.



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PRIMARY EXAMINER